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PATENT
(5500-68500/TT4418)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/061, 671

Filed: February 1, 2002

Inventor(s):

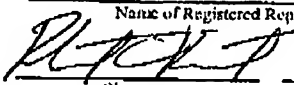
Michael A. Filippo

Examiner: Wang, Albert C.

Group/Art Unit: 2115

Atty. Dkt. No: 5500-68500

Title: Apparatus and Method for
Selective Clock Control to
Reduce Power Consumption
in an Integrated Circuit

**** CERTIFICATE OF FACSIMILE ****	
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Robert C. Kowert	
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	July 29, 2005
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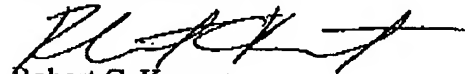
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Respectfully submitted,


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